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# Sequential Logic Circuits Using Spatial Wavefunction Switched (SWS) FETs

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# **Sequential Logic Circuits Using Spatial Wavefunction Switched (SWS) FETs**

Neeraja Jagadeesan

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# **APPROVAL PAGE**

Master of Science Thesis

## **Sequential Logic Circuits Using Spatial Wavefunction Switched (SWS) FETs**

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## **Abstract**

In this thesis, sequential logic circuits have been implemented using spatial wavefunction-switched field-effect transistor (SWSFET). The spatial wavefunction-switched field-effect transistor (SWSFET) is one of the promising quantum well devices that transfers electrons from one quantum well channel to the other channel based on the applied gate voltage. This eliminates the use of more transistors as we have coupled channels in the same device operating at different threshold voltages. This feature can be exploited in many digital integrated circuits thus reducing the count of transistors which translates to less die area. The simulations of basic sequential circuits like SR latch, D latch are presented here using SWSFET based binary logic gates. The circuit model of a SWSFET was developed using Berkeley short channel IGFET model (BSIM3) in Cadence simulator. Multi-valued logic is an interesting aspect of SWSFET as it is capable of having multiple channels. Since each channel has a threshold voltage and can be selected by applying the appropriate gate voltage, SWSFET offers several design possibilities with more than just two states. In this thesis, a quaternary D flip flop is presented with simulations done using VHDL Behavioral model. The number of transistors is reduced by nearly 80% when compared to the conventional CMOS circuits. By using quaternary to binary and binary to quaternary conversion circuits, it is possible to integrate the quaternary circuits with the existing binary circuits.

## 1. Introduction

The need for high speed, power efficient and compact integrated circuits has led to the invention of novel quantum devices like quantum dot gate FETs (QDGFETs), quantum dot channel FETs (QDCFETs) [1,2] and spatial wavefunction-switched FETs (SWSFETs) [3]. These devices use semiconductor materials like Ge, InGaAs and high-k lattice matched layers as gate insulator which reduces the leakage current as opposed to the regular SiO<sub>2</sub> gate oxide in the sub-12-nm regime. Multi-state behavior has also been seen in these devices which can be utilized in multi-valued logic circuits [4].

As an alternative technology to the existing CMOS technology, several circuit demonstrations are needed to prove the viability of SWSFETs as promising building blocks for energy efficient digital circuits. Chapter 2 introduces the SWSFET device that was first developed and patented by Jain et al illustrating the two well and four well structures along with the quantum mechanical simulations [6]. The transfer of charge between wells, channel charge density and experimental capacitance voltage characteristics are shown in this chapter.

The logic gates which are essential for any digital system have been designed using SWSFETs. Chapter 3 shows the circuit designs of Inverter, NAND, NOR using lesser number of SWSFETs. The simulations were carried out in Cadence and the truth tables were verified. The combination of logic gates can be used in the implementation of sequential logic circuits. The basic latches and edge triggered flip flops have been demonstrated in Chapter 4. This in turn can be used to build more complex sequential circuits such as shift registers, counters and memory devices. The functionality was verified using VHDL behavioral simulation.

Quaternary logic circuits have been designed and simulated using SWSFETs [5]. Quantum well devices allow us to realize applications that are beyond the capability of the conventional CMOS technology. This gives impetus to simulate circuits and understand the potential of new quantum devices. Chapter 4 demonstrates a quaternary flip flop and integration with binary logic. Finally a comparison is done with CMOS technology and suggestions for future work are discussed.

## 2. Spatial Wavefunction Switched (SWS) FETs

SWSFET devices are based on the idea of incorporating asymmetric quantum well channels so that the electron wavefunctions switch from one well to the other as a function of the gate voltage.

### 2.1 SWSFET: Structure and Operation

III-V compounds are used in the asymmetric channels of SWSFET where wells are made of InGaAs with alternating barriers of AlInAs on p-InGaAs that is grown on InP substrate. InGaAs which has carrier mobility higher than that of Silicon is used in the SWSFET configuration to provide faster switching feature in the device [6].

II-VI gate dielectric ZnMgSeTe is used in placed of the amorphous SiO<sub>2</sub> or HfO<sub>2</sub>. “The heteroepitaxial barrier stack can stabilize the threshold voltage by minimizing the interface charge at the barrier-channel interface. The magnesium incorporation increases the energy barrier but introduces dislocation that can leak charge. The ZnS and ZnSe layers have a lower bandgap but a lower dislocation density to assist with gate leakage prevention” [8].

#### 2.1.1 Two well SWSFET

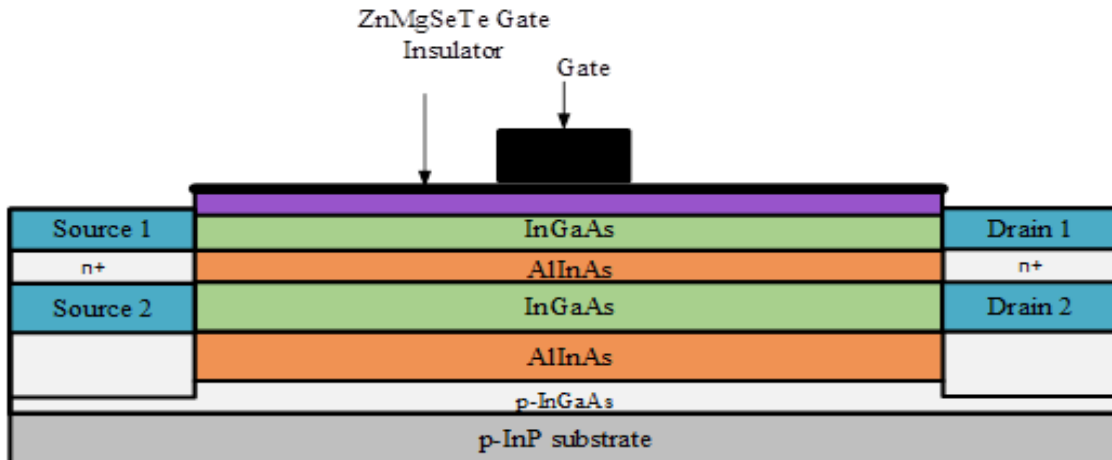


Fig 1. Two well InGaAs-AlInAs SWSFET with twin Source and Drain.

Figure1 shows the cross-sectional view of a two well SWSFET. The asymmetric dimensions of the two wells determine the way the channels conduct electrons. The lower well is comparatively larger than the upper well so as the gate voltage applied increases ( $V_G > V_{TH2}$ ), the electrons appear first in the bottom well (well 2). The electron wavefunctions spatially switch from the lower well to the upper well (well 1) with an applied voltage ( $V_G > V_{TH1}$ ).

### 2.1.2 Four well SWSFET

The four channel SWSFET configuration with common drain is shown in Figure 2. Each channel in this device has a different threshold voltage which makes it viable for quaternary logic. While the twin channel device is used to implement binary logic, the quaternary logic holds huge promise and offers several alternatives to more complex design systems.

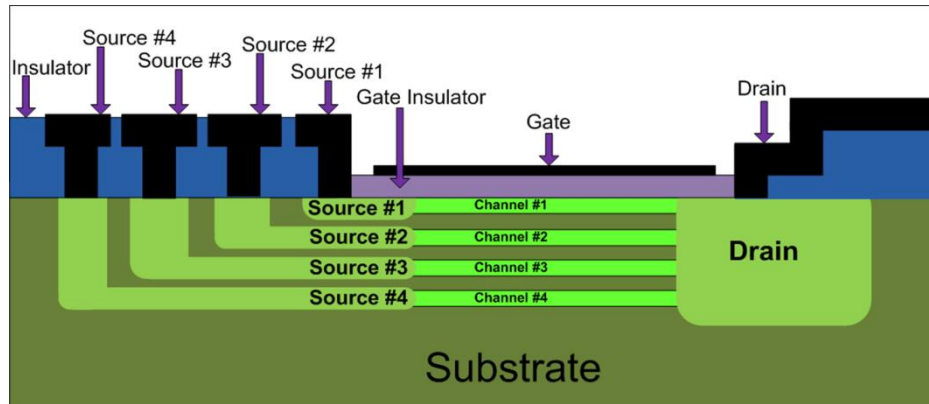


Fig 2. Four channel SWSFET with common drain configuration [7]

## 2.2 SWSFET Characteristics and Simulations

The quantum simulations showing the transfer of charges between the two wells, channel charge density as a function of gate voltage are presented in Figure 3. The peak seen in the C- V characteristics shows the transfer of electrons from well 2 to well 1 [6].

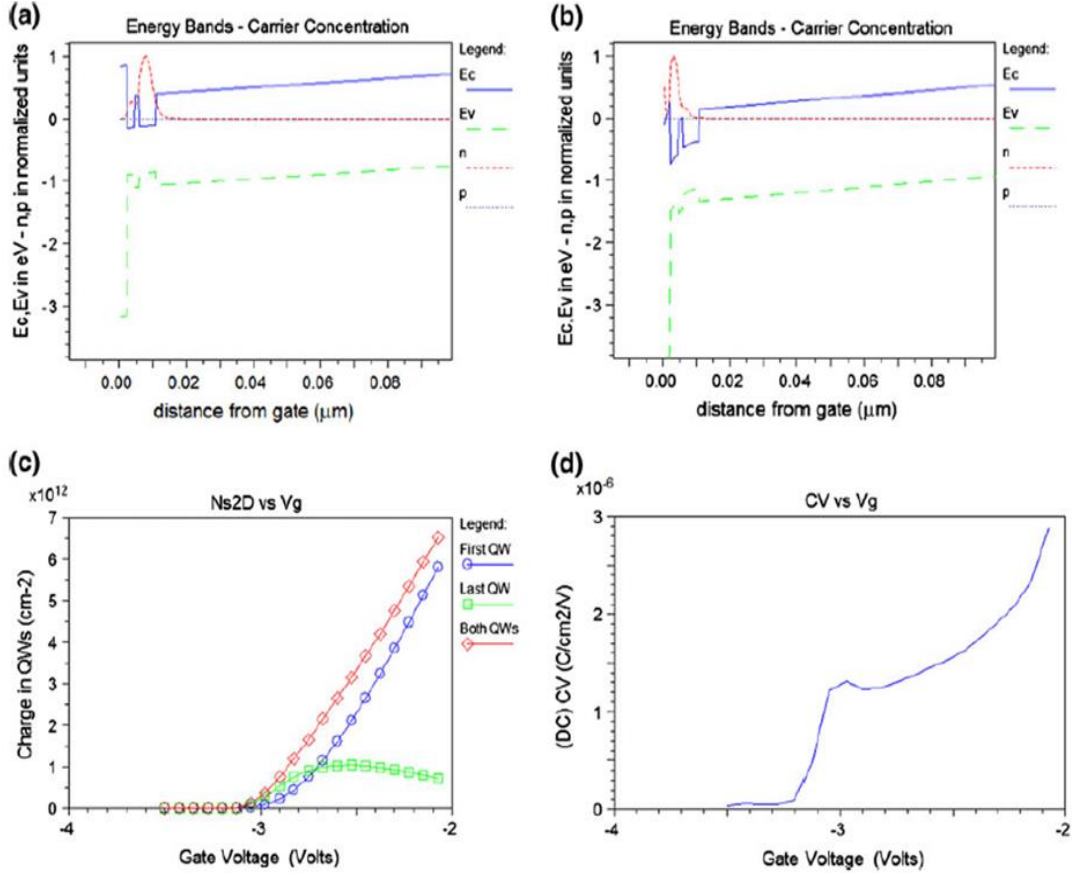


Fig 3. Simulations of the two well SWSFET device [6]

The experimental capacitance voltage (C-V) plot for a fabricated two quantum well InGaAs - AlInAs MOS capacitor can be seen in Fig 4. The C-V plot at 10 kHz for an InGaAs SWS sample (#1962) having two quantum wells can be seen in Fig 4(a). The accumulation region shows the presence of two threshold voltages corresponding to the two quantum wells. “The peak on the left (at approximately - 3.2V) is due to the holes first appearing in the lower well W2 and subsequently transferring to the upper well W1 as we move away from threshold towards accumulation”[6]. Fig4(b) shows the C-V plot for a different InGaAs two-well sample (#1965). Here, the peaks are more distinct in the accumulation region.

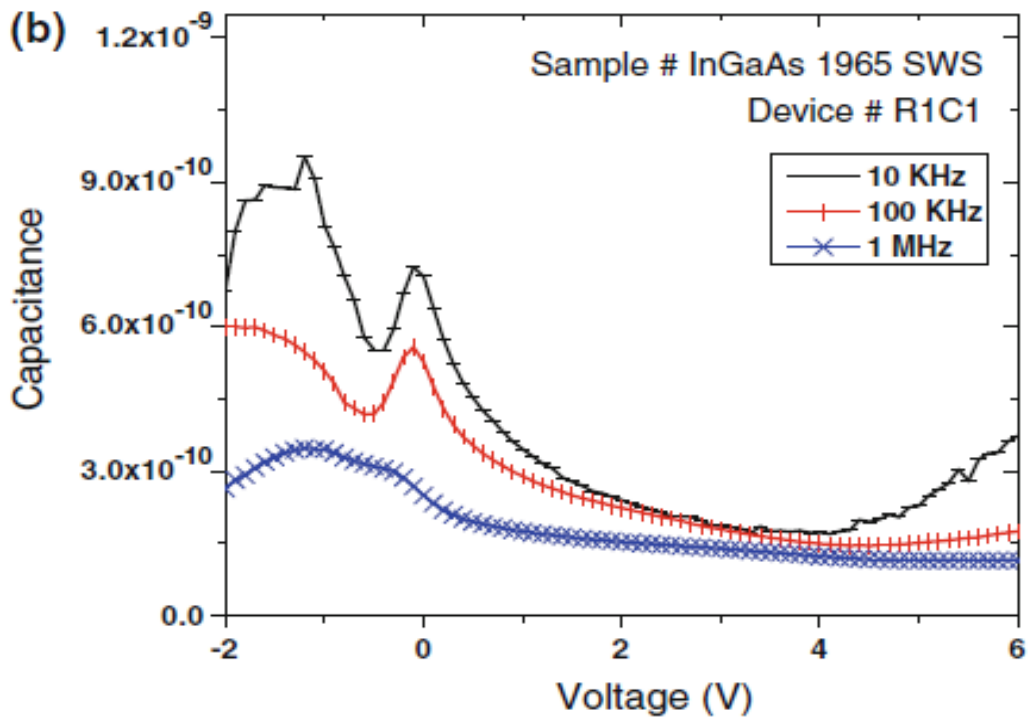
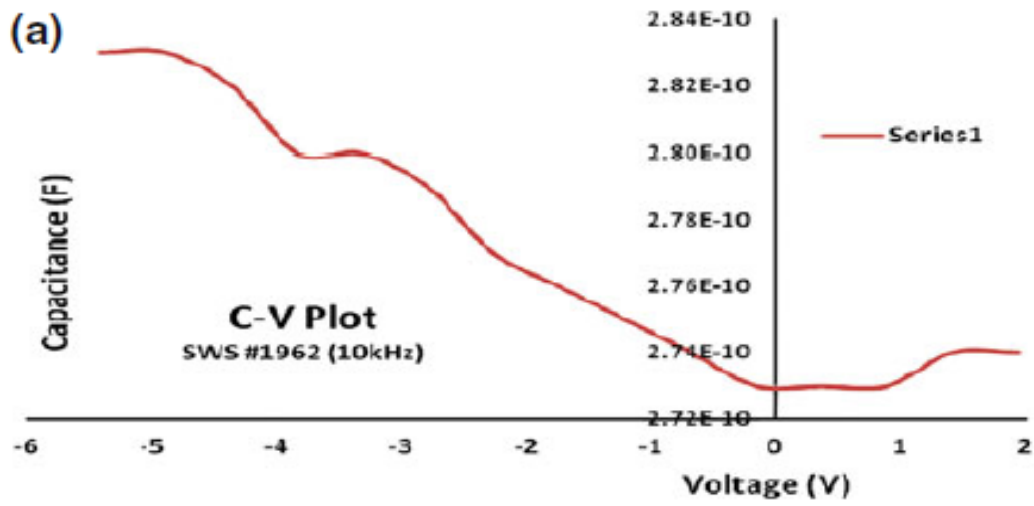


Fig 4. Experimental capacitance–voltage characteristics of a two-well SWS device [6]

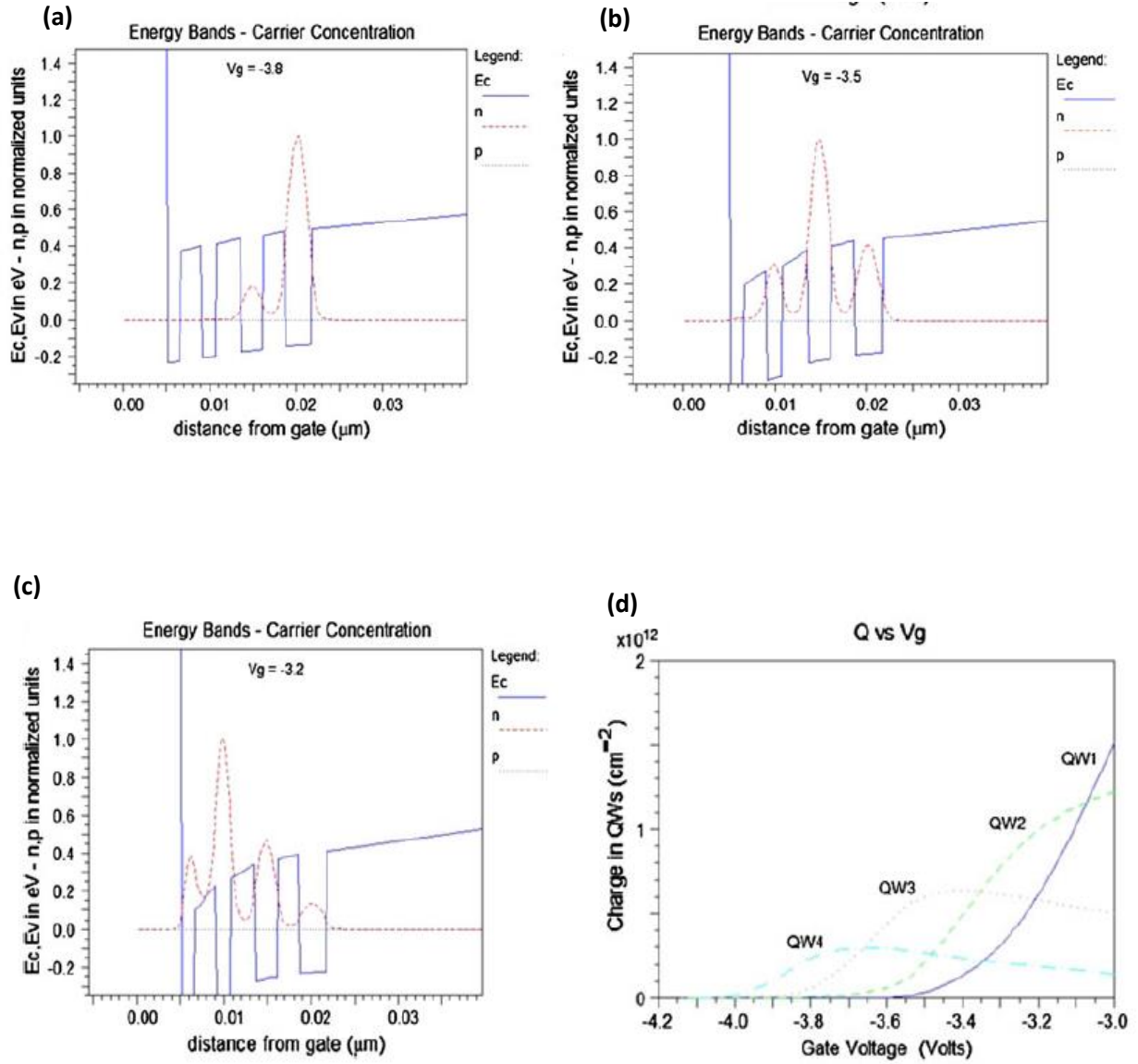


Fig 5: Simulations of four well SWSFET device [7]

As a function of gate voltage the transfer of charge between the wells can be seen in Fig 5(a)-(c). When  $V_g = -3.8$  V the SWS wavefunction is present in W4 then switches to W3 for  $V_g = -3.5$  V and SWS wavefunction finally is seen in W2 for an increased gate voltage of  $V_g = -3.2$  V. The charge density plot as a function of gate voltage in various quantum wells can be seen in Fig 5(d).



### 3. SWSFET Logic gates

By taking advantage of the twin channel feature, some of the basic logic gates like Inverter, NOR and NAND that serve as the fundamental building blocks of any digital system have been designed. The logic cells use the n-channel type SWSFETs and work on binary logic. The common uses of combinational logic gates are in half adders, full adders, multiplexer, demultiplexer, encoder, decoder type circuits. SWSFET based logic gates can be used to design efficient circuits using less number of transistors. In SWSFETs, the gate voltage is similar to the select signal of a multiplexer and the data inputs connected to the sources of the channels can be selectively chosen using the gate signal. Different logic states are assigned to the device according to the current levels in the channels. So the device provides four states 00, 01, 10, 11 corresponding to the wavefunction being OFF (00), in well W2 (01), in Well 1 (10) and in both wells W2-W1 (11) [6]. The state assignments can be used in the implementation of efficient logic circuits. Quaternary logic gates have been designed and simulated using SWSFETs that drastically reduced the count of transistors in comparison with the CMOS logic cells [7].

#### 3.1 SWSFET Inverter

The Inverter design uses two n-channel SWSFETs [1]. The twin source and drain configuration is operated in such a way that either of the two wells is chosen according to the applied input voltage. Fig 6 shows the connections of SWS1 and SWS2 with the conducting paths marked in dotted lines. The lower wells are designated as S2, D2 and upper wells as S1, D1 respectively. When the input voltage  $V_{in}$  is 0, the lower wells of the two SWSFETs are in the conducting mode. The D2 of SWS2 is a floating node whereas D2 of SWS1 connects the output to  $V_{dd}$  thus giving logic '1'. When the input voltage  $V_{in}$  is 1, the upper wells of the two SWSFETs are in the conducting mode. The D1 of SWS1 is a floating node whereas D1 of SWS2 connects the output to Gnd thus giving logic '0'.

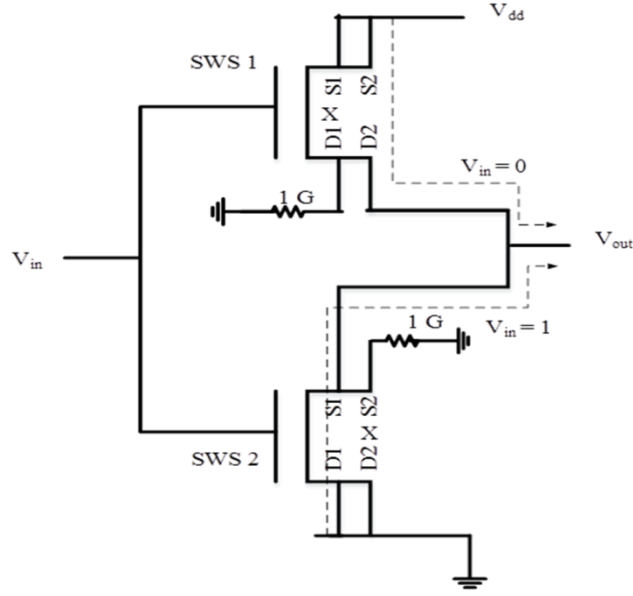


Fig 6. Inverter design using SWSFETs.

### 3.2 SWSFET NOR gate

The NOR design uses one SWS inverter and one n-channel SWSFET. Figure 7 shows the connections of the circuit. Input A is given to the inverter and Input B is given to SWS3. The lower channel of SWS3 is connected to the output of the inverter so whenever Input B is logic '0', the inverted value of Input A is propagated to the output. The upper channel of SWS3 is connected to Gnd so whenever Input B is logic '1', the output is connected to Gnd giving logic '0' irrespective of Input A.

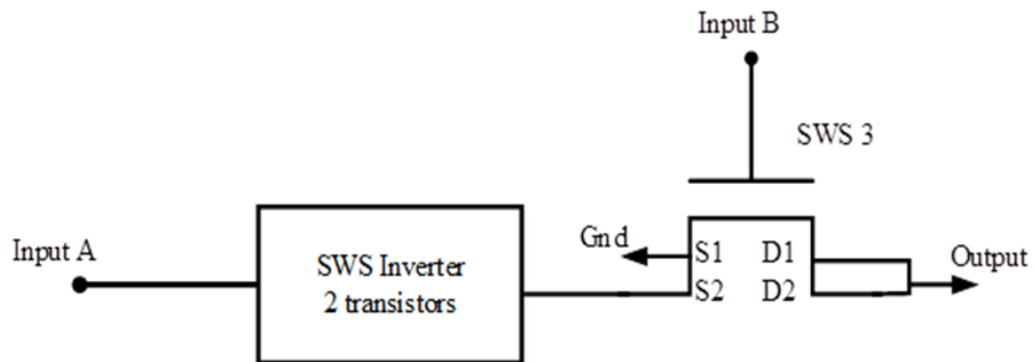


Fig 7. Schematic diagram of SWSFET NOR gate.

### 3.3 SWSFET NAND gate

The NAND design uses one SWS inverter and one n-channel SWSFET. Figure 8 shows the connections of the circuit. Input A is given to the inverter and Input B is given to SWS3. The upper channel of SWS3 is connected to the output of the inverter so whenever Input B is logic '1', the inverted value of Input A is propagated to the output. The lower channel of SWS3 is connected to Vdd so whenever Input B is logic '0', the output is connected to Vdd giving logic '1' irrespective of Input B.

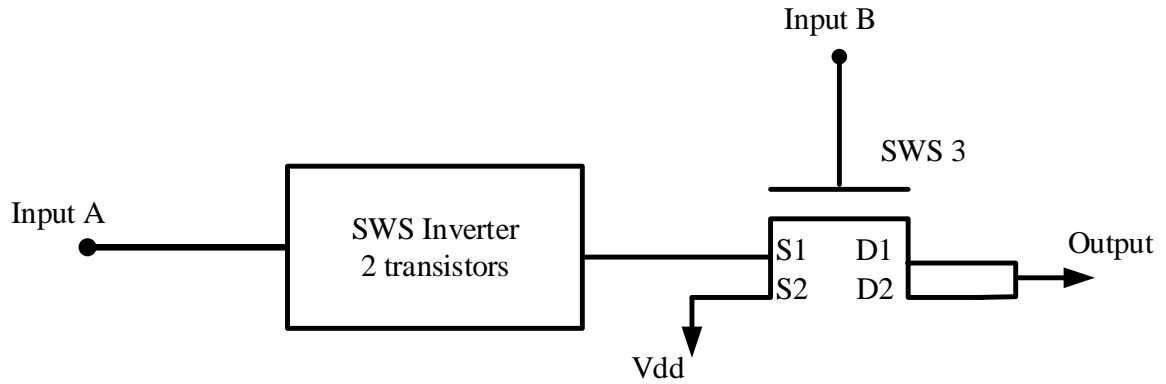


Fig 8. Schematic diagram of SWSFET NAND gate.

### 3.4 SWSFET circuit model

The circuit model of a SWSFET was developed using Berkeley short channel IGFET model (BSIM 3). The two SWSFET channels are represented by two conventional transistors with each one having a different threshold voltage which is characteristic of a SWSFET. For the two channel SWSFET, the threshold voltage of the lower channel is 0.5V and the upper channel is 0.7V as seen in Fig 9.

The drain current for MOSFET is given by Eq(1) and this equation can be applied to SWSFET to represent the drain current in well 1 and well 2 given by Eq.(2) and Eq.(3) respectively by S.Karmakar [9]. Simulations were done using Cadence tool and the results of the logic design simulations using SWSFET are in accordance with the truth tables.

$$I_{DS} = \left(\frac{W}{L}\right) C_{OX} \mu_n \left( (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (1)$$

$$I_{DS-\text{well } 1} = \left(\frac{W}{L}\right) C_{OX} \mu_n \left( (V_{GS} - V_{th1}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (2)$$

$$I_{DS-\text{well } 2} = \left(\frac{W}{L}\right) C_{OX} \mu_n \left( (V_{GS} - V_{th-\text{well}2}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (3)$$

The threshold voltage in well2  $V_{th-\text{well } 2}$  can be expressed as

$$V_{th-\text{well } 2} = \begin{cases} V_{th2} & \text{when } V_{GSeff} < V_{qL} \\ V_{th2} + \alpha (V_{GSeff} - V_{qL}) & \text{when } V_{GSeff} > V_{qL} \end{cases} \quad (4)$$

Where  $\alpha$  is the matching parameter and is given by

$$\alpha = \frac{V_{GS} - V_{qL}}{V_{q1} - V_{qL}} \quad (5)$$

Here  $\alpha$  controls the slope of the characteristics.

The effective gate voltage can be expressed as

$$V_{GSeff} = V_{GS} - V_{PolyEff} \quad (6)$$

where

$V_{th-\text{well}2}$  developed threshold voltage of well 2

$V_{th2}$  threshold voltage of well 2

$V_{th1}$  threshold voltage of well 1

$V_{qL}$  is the transition voltage

$V_{q1}$  is the voltage corresponding to peak current in well 2

$\alpha$  is a matching parameter

$V_{GS}$  is the gate-source voltage

$V_{PolyEff}$  is the voltage drop in the Poly Si gate

$V_{GSeff}$  is the effective gate-source voltage

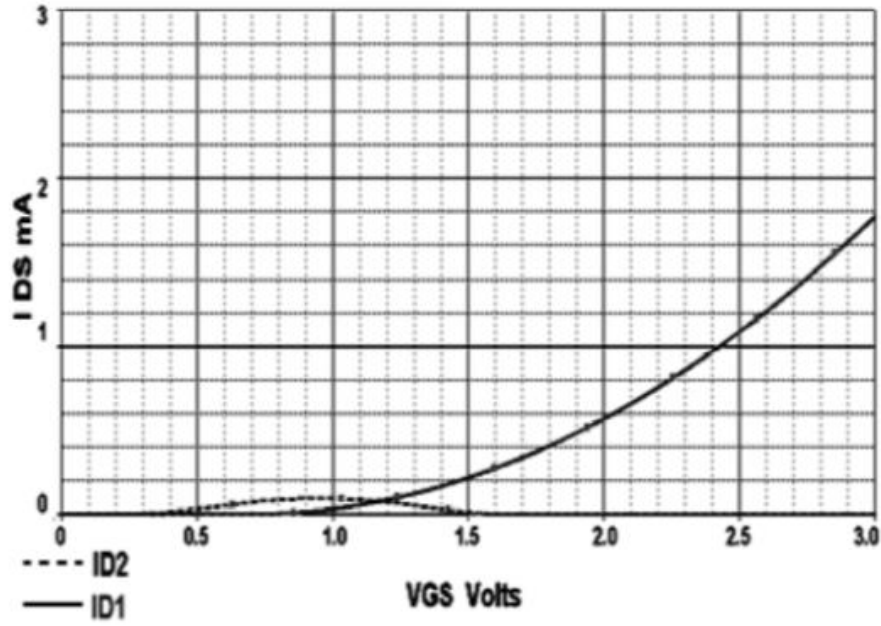


Fig 9. SWSFET  $I_{DS}$ - $V_{GS}$  Characteristics

Table 1. SWSFET circuit model parameters

Parameter	Value
L	5.0 $\mu\text{m}$
W	10 $\mu\text{m}$
V <sub>th2</sub>	0.5 V
V <sub>th1</sub>	0.7 V
V <sub>qL</sub>	0.6 V
V <sub>q1</sub>	1.5 V
VDD	3.0 V

The SWSFET circuit was modelled with parameters as shown in Table 1 to verify its functionality in different logic circuits. The functionality of this SWSFET model can be compared to 25 nm channel length SWSFET model reported earlier [5].

## 4. Sequential Circuits

Sequential circuits are made up of a block of combinational logic circuits along with a feedback component that gives the state information. In this type of logic the output depends not only on the latest inputs, but also on the condition of earlier inputs. So they implicitly contain memory elements.

These circuits are usually two state or bistable devices which can have its output set in one of the two basic states, a logic level “1” or a logic level “0” and will remain “latched” in this current state until some other input trigger pulse is applied which will cause a change of state again. The trigger pulse or signal is a clock signal that determines what comes one after the other in a sequential circuit. Simple sequential logic circuits can be constructed from basic circuits such as flip flops, latches and counters. These basic circuits can be made by simply connecting together logic gates like NOT, NAND Gates and NOR Gates in a certain combinational way to obtain the required sequential circuit.

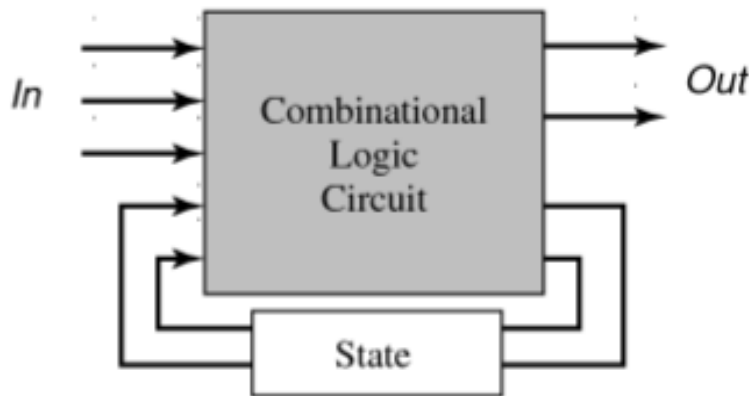


Fig 10. Block diagram of a Sequential logic circuit

### 4.1 Timing metrics

An important aspect of sequential logic circuit is the timing parameter namely set-up time, hold time and propagation delay associated with the proper functioning of the circuit as seen in Fig 11 [10]. “The set-up time ( $t_{su}$ ) is the time that the data inputs (D input) must be valid before the clock transition (this is, the 0 to 1 transition for a positive edge-triggered register). The hold time ( $t_{hold}$ ) is the time the

data input must remain valid after the clock edge. Assuming that the set-up and hold-times are met, the data at the D input is copied to the Q output after a worst-case propagation delay (with reference to the clock edge) denoted by  $t_{c-q}$  [10].

If the worst-case propagation delay of the logic equals  $t_{plogic}$  and its minimum delay (contamination delay) is  $t_{cd}$  then the minimum clock period  $T$ , required for proper operation of the sequential circuit is given by Eq(7) [10].

$$T \geq t_{c-q} + t_{plogic} + t_{su} \quad (7)$$

The hold time of the register imposes an extra constraint for proper operation given by Eq(8) [10]

$$t_{cdregister} + t_{cdlogic} \geq t_{hold} \quad (8)$$

$t_{cdregister}$  is the minimum propagation delay (or contamination delay) of the register.

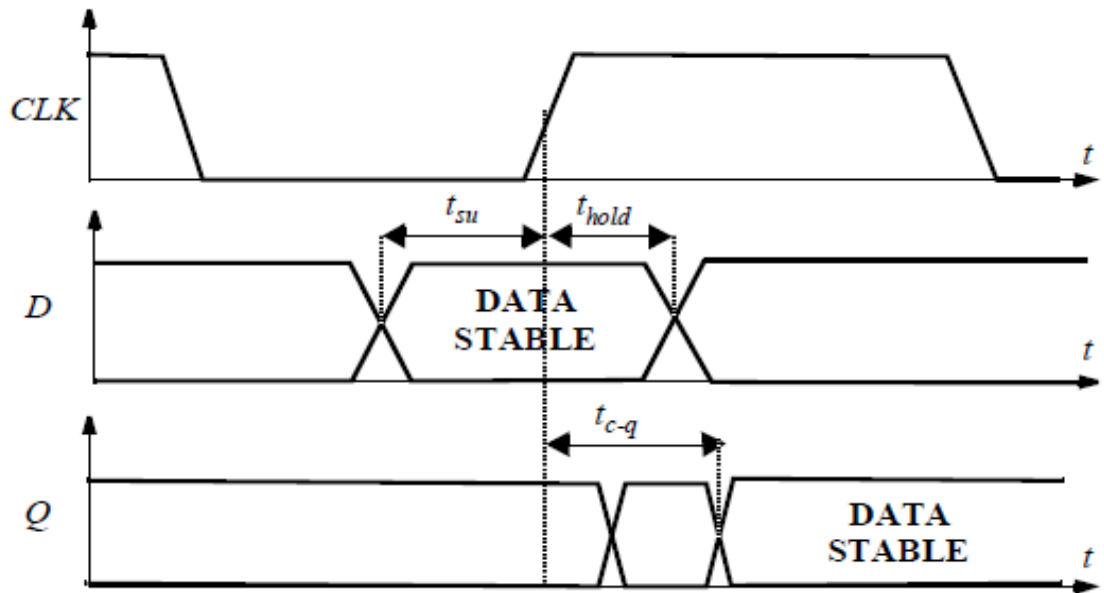


Fig 11. Timing metrics of a synchronous register [10]

It is necessary to reduce the impact of timing parameters in a register. This can be done by having a very-low logic depth and having the register propagation delay and set-up time account for a significant portion of the clock period [10].

## **4.2 Latches and Flip flops**

Latches are level sensitive which means the D input is seen at the output as long as the clock is high or low in a positive or negative latch respectively. This is called the transparent mode of the latch and any change in the D input is passed to the Q output. When the next clock transition occurs, the latch stops sampling the input data and the previous state of the output is held stable. This is the hold mode of the latch. The inputs must be stable for a short period around a falling or rising edge of the clock to meet the set-up and hold requirements [10].

Unlike the latches, flip flops are edge-triggered devices. The input is sampled only when the clock makes a low to high or high to low transition in a positive edge triggered or negative edge triggered flip flop respectively. The flip flops are constructed using the basic latches by cascading two latches to form a master-slave configuration. If the master is a positive latch and slave is a negative latch then it is called negative edge-triggered flip flop.

## **4.3 SR Latch**

The SR latch is a type of memory element with inputs Set (S) and Reset (R) and outputs Q and its complementary  $\bar{Q}$ . The circuit is implemented using SWSFET based NOR logic gates. This being one of the basic sequential logic circuits, several other latches and flip flops can be constructed using this SWSFET based circuit. When  $S=0$  and  $R=1$  the output Q is reset to zero and  $\bar{Q}$  is logic '1'. In the case of set condition when  $S=1$  and  $R=0$  the output Q is set to logic '1' whereas  $\bar{Q}$  goes to logic '0'. But there is no change in outputs Q and  $\bar{Q}$  when both  $S=0$  and  $R=0$  which is called the hold condition. The last condition when  $S=1$  and  $R=1$  both outputs go to logic '0' which is a forbidden state.



Figure 12 shows the circuit diagram. This is asynchronous as it does not have a clock signal.

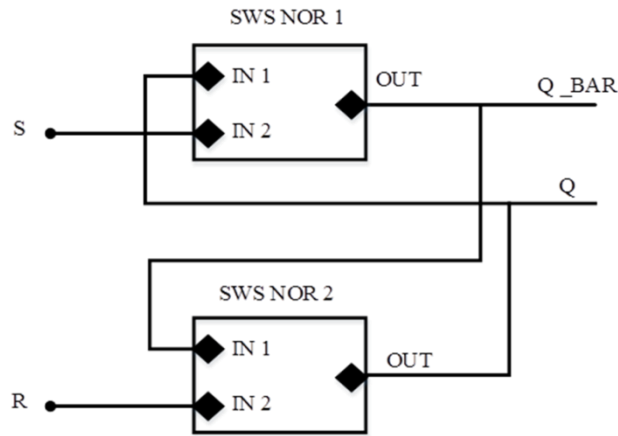


Fig 12. SR Latch circuit using SWSFET NOR gates.

Table 2. Truth table of SR Latch

S	R	Q	Q_BAR
0	0	No	change
0	1	0	1
1	0	1	0
1	1	0	0

#### 4.4 D Latch

The D Latch design uses two SWSFET inverters. This is a synchronous circuit with a clock signal so the output changes only when a clock event or transition occurs. Unlike the SR latch the illegal condition is avoided such that Q and Q\_bar are complementary to each other under all input conditions. The clock signal is given to the gate of a twin channel SWSFET with common drain configuration where each of the channels is selected by a gate input of logic '0' and logic '1' respectively.

This simple design when implemented using CMOS, NMOS only pass transistors are used to clock in the D input to the first inverter and control the feedback path. So when clock is high, a degraded high voltage of  $V_{DD}-V_{Tn}$  is passed to the input of the first CMOS inverter. This impacts both noise margin and the switching performance, especially in the case of low values of  $V_{DD}$  and high values of  $V_{Tn}$  [10]. It causes static power dissipation in first CMOS inverter. Since there is a threshold voltage drop in the NMOS pass transistor, the resulting output voltage is  $V_{DD}-V_{Tn}$ . This is the maximum input voltage given to the CMOS inverter and the PMOS device of the inverter is not turned off, resulting in a static current flow.

#### 4.4.1 Positive D Latch

The input D is applied to the source of channel 1 and the feedback input is given to the source of channel 2 to store the previous data. When the clock state is '1' all the changes in input D is seen at the output and when the clock goes to '0' the feedback component is activated and latches the output Q at either logic '0' or '1'. Depending on the voltage applied the corresponding channel is activated and connected to the output. The device functions as a level sensitive positive D latch.

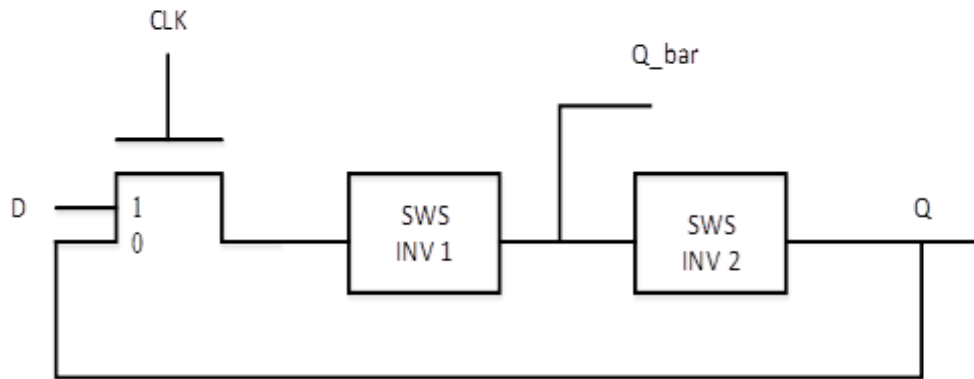


Fig 13. Positive D latch circuit using SWSFET

Table 3. Truth table of D Latch

D	CLK	Q	Q_BAR
X	0	Hold	State (no change)
0	1	0	1
1	1	1	0

#### 4.4.2 Negative D Latch

The input D is applied to the source of channel 0 and the feedback input is given to the source of channel 1 to store the previous data. When the clock state is '0' all the changes in input D is seen at the output and when the clock goes to '1' the feedback component is activated and latches the output Q at either logic '0' or '1'. Depending on the voltage applied the corresponding channel is activated and connected to the output. The device functions as a level sensitive negative D latch.

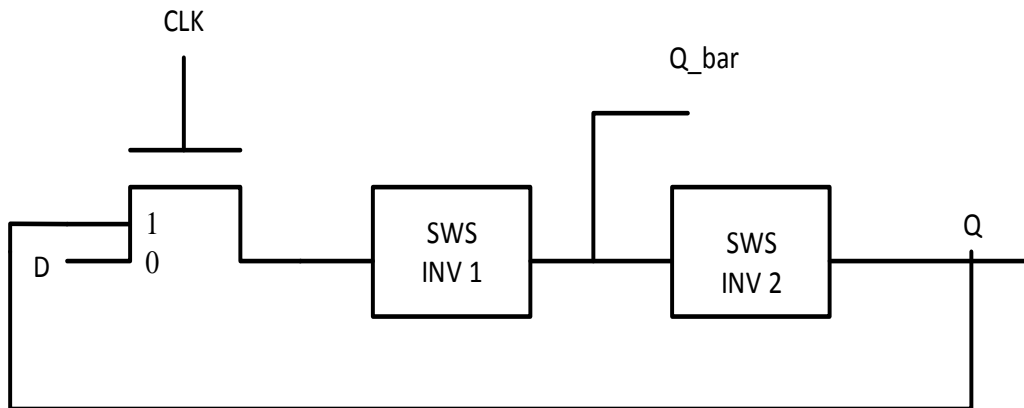


Fig 14. Negative D latch circuit using SWSFET

## 4.5 Simulations

The simulation of SR Latch was done in Cadence using the SWSFET circuit model developed using Berkeley short channel IGFET model (BSIM 3). The functionality is similar to that of a CMOS equivalent circuit and the results are shown in Fig 15. For the simulation of D latch, VHDL behavioral model was used. The functionality of the D latch can be seen in Fig 16 and 17.

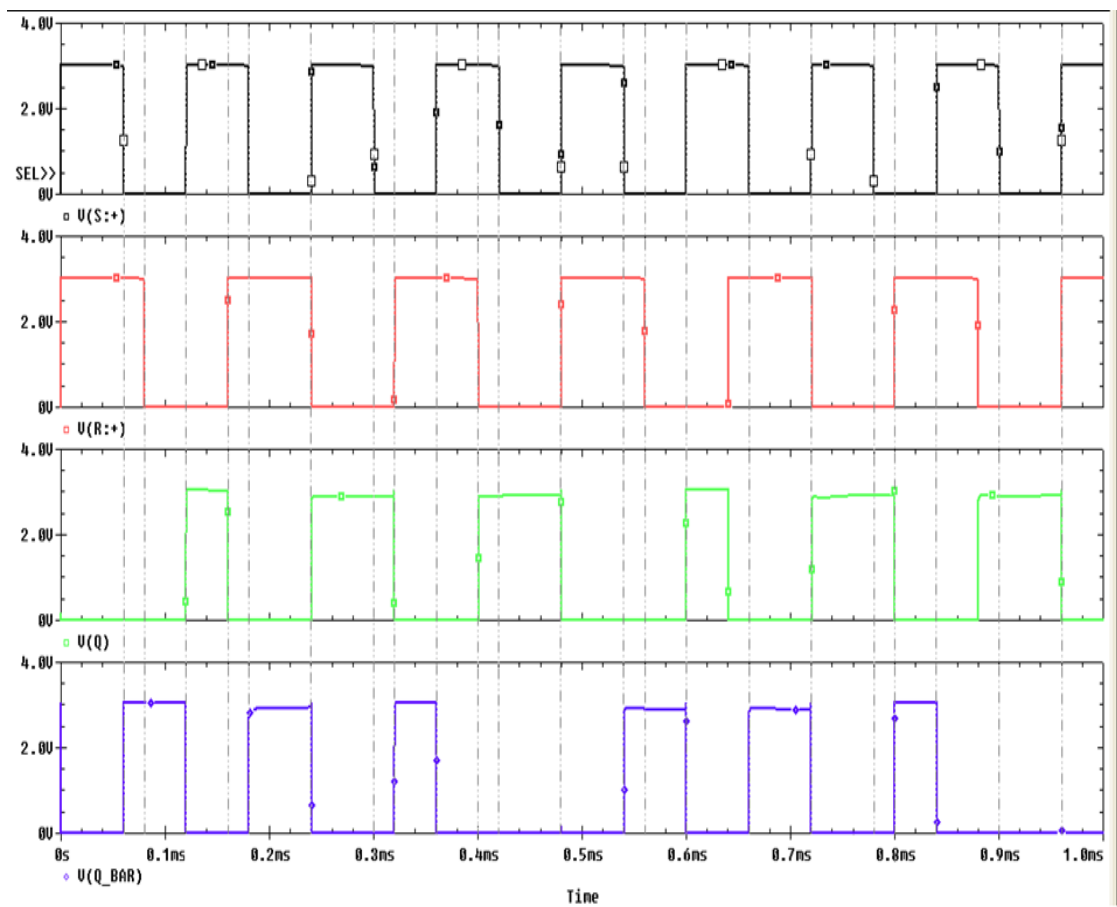


Fig 15. Simulations of SR Latch using SWSFET NOR logic gates

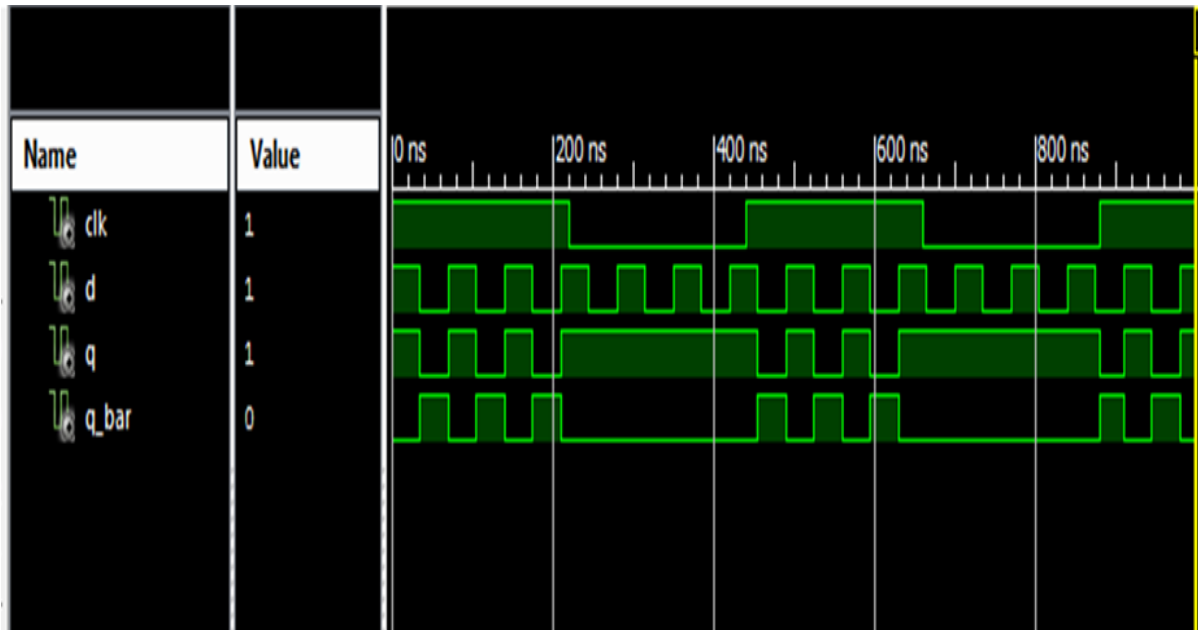


Fig 16. Behavioral simulation of SWS based positive D latch circuit

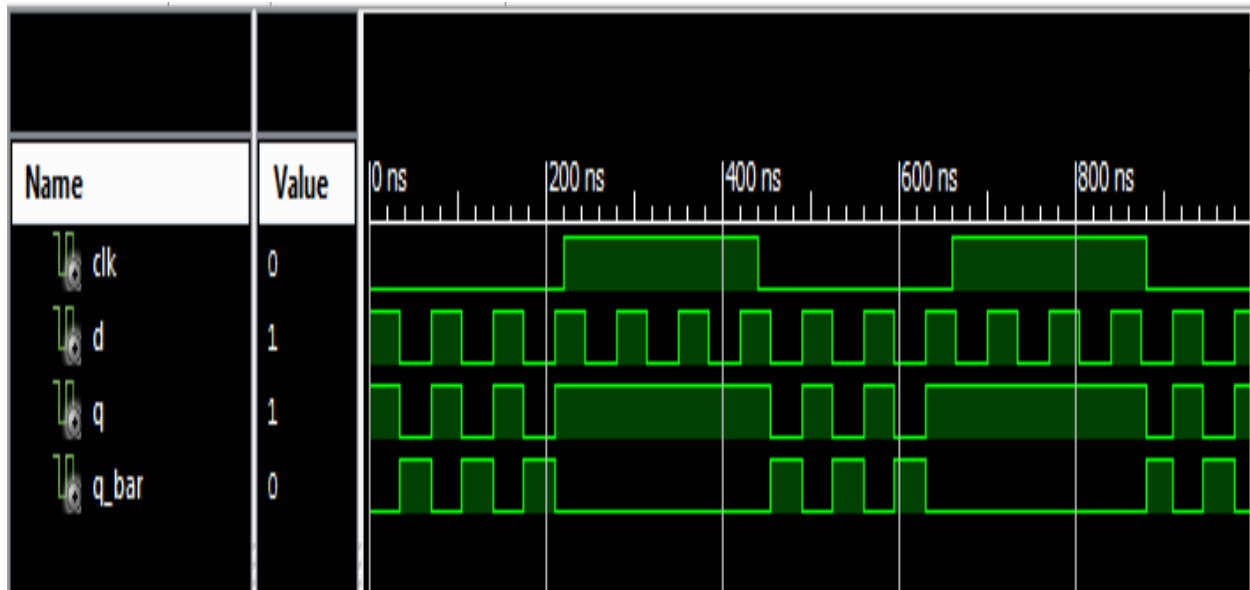


Fig 17. Behavioral simulation of SWS based negative D latch circuit

## 5. Quaternary Logic

The multiple channels in SWSFETs can be used in designing circuits with more than two states that is not possible using the conventional single channel CMOS transistors. Quaternary logic designs previously done using SWSFET prove the capability of the device as multi-bit logic cells [5]. The logic gates can process two bit operations at a time whereas the equivalent CMOS binary logic circuit will require four times as many transistors as used in the SWSFET design [7]. The four quaternary levels 0, 1, 2 and 3 can be represented in two bit binary form as 00, 01, 10 and 11 states. “Therefore at any node in an electronic circuit a quaternary logic could be converted to binary levels and vice-versa, given the availability of the right number of binary bits” [7].

### 5.1 Quaternary inverter

The NOT operation is done on the novel quaternary logic and its truth table is presented in Table 4 [7]. The logical block is shown in Fig 18 and it can be seen that only one SWSFET is used to perform the quaternary NOT operation. In case of CMOS binary logic, four transistors would be needed.

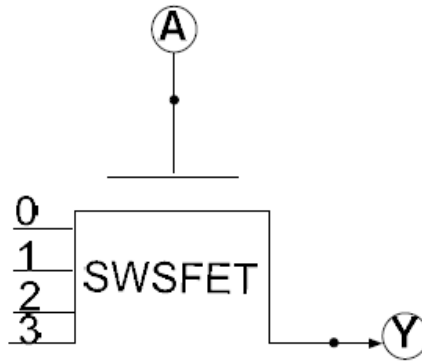


Fig 18. Quaternary NOT gate [5,7]

Table 4. Truth table of NOT gate [7]

$A(A_1, A_2)$	NOT $A = Y(Y_1, Y_2)$
0(00)	3(11)
1(01)	2(10)
2(10)	1(01)
3(11)	0(00)

## 5.2 Quaternary D Flip flop

Multi-valued flip flops have been researched for quite some time now [11-13]. Ternary flip flops have been reported earlier using resonant tunneling diode (RTD) [20]. Two latches using SWSFET based quaternary inverters are cascaded to form the master slave flip flop circuit. The quaternary inverter is designed by the selection of appropriate sources at different gate voltages for a single SWSFET [5]. The two CLK driven SWSFETs turn on the latches in such a way that the master stage is transparent during the high phase of the clock and the D input is passed to the master stage output  $Q_M$ . So it behaves like a positive latch. During this period, the slave stage is in the hold mode, keeping its previous value using feedback. On the falling edge of the clock, the master slave stops sampling the input, and the slave stage starts sampling. During the low phase of the clock, the slave stage which is a negative latch samples the output of the master stage ( $Q_M$ ), while the master stage remains in a hold mode. The value of Q is the value of D right before the falling edge of the clock, achieving the negative edge-triggered effect.

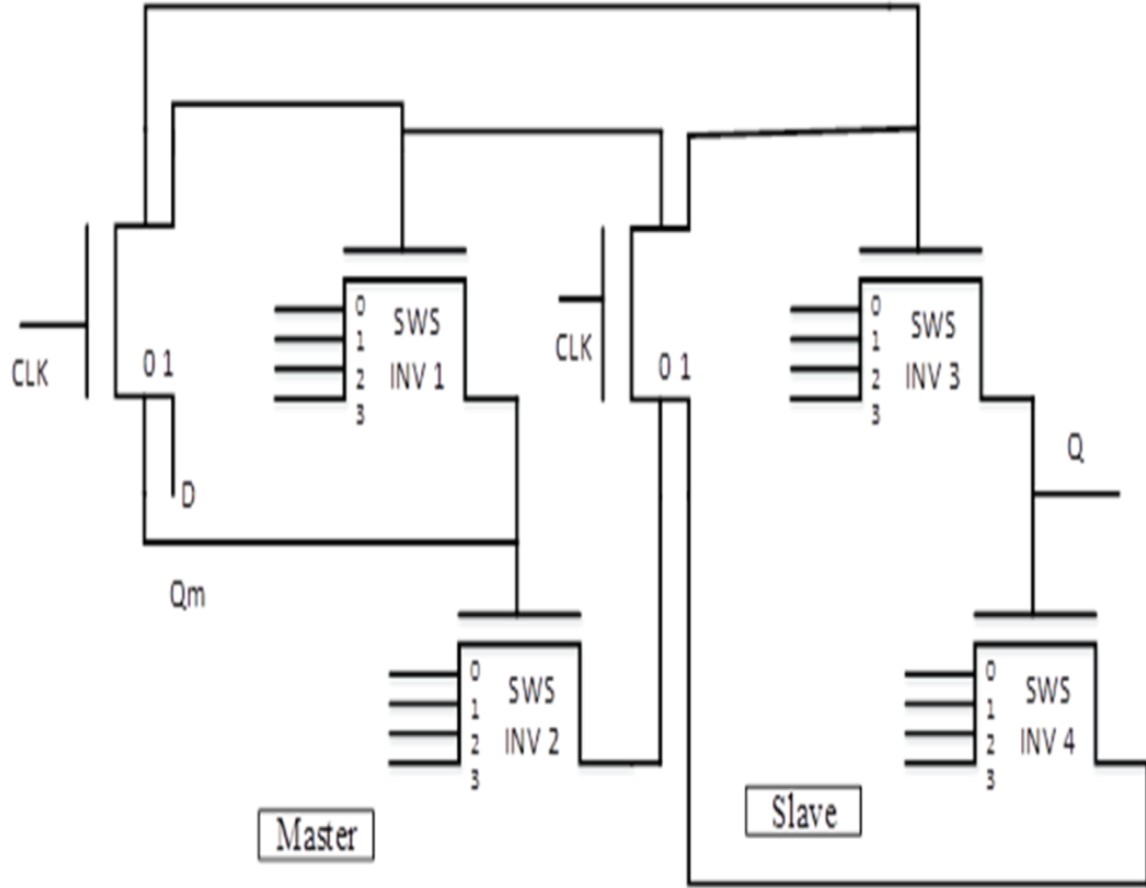


Fig 19. Quaternary negative edge-triggered D flip flop using four channel SWSFET

### 5.2.1 Simulations

The quaternary inverter was simulated using the Advanced Design Simulator (ADS) tool with Berkeley short-channel insulated gate field-effect transistor (IGFET) model (BSIM) equivalent channel models for SWS FETs with channel length of 25 nm [5]. Figure 20(b) gives the output waveform for an SWS FET-based inverter for the input waveform shown in Figure 20(a). The circuit modelling was done using four conventional transistors each one having a different threshold voltage which is characteristic of a SWSFET device. The four voltages corresponding to the four channels are  $V_{cc}$ ,  $0.66 V_{cc}$ ,  $0.33 V_{cc}$  and Gnd.



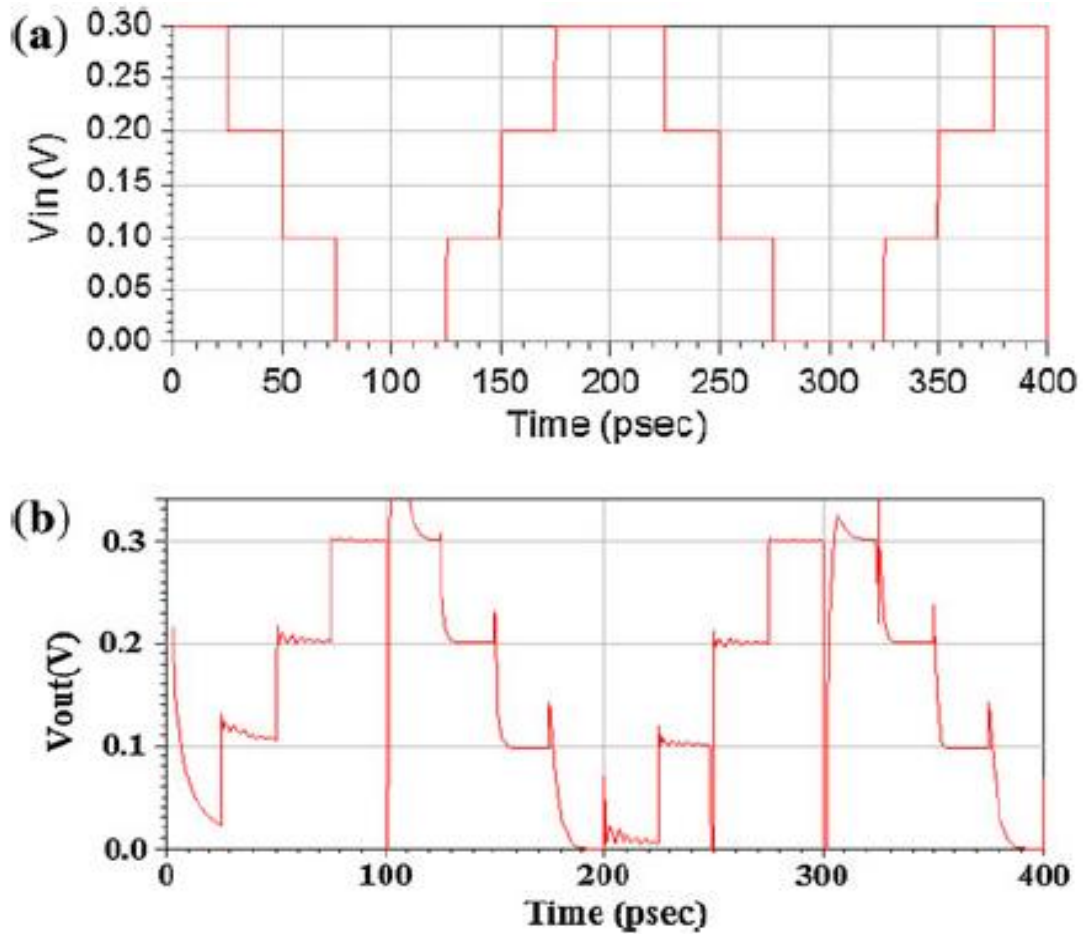


Fig 20. Inverter Simulation (a) Input versus time waveform (b) Output versus time waveform [5]

The simulation shown in Figure 21 was done using VHDL behavioral model to demonstrate the functionality of a quaternary flip flop. The output of the master stage is shown as 'qm' and the final output from the slave stage is 'q'. In the VHDL simulation as seen below, the two bit binary equivalent of the analog voltage levels was implemented in the circuit for ease of usage and understanding. Similarly simulations were verified for a positive edge triggered flip flop by cascading a negative latch and a positive latch.

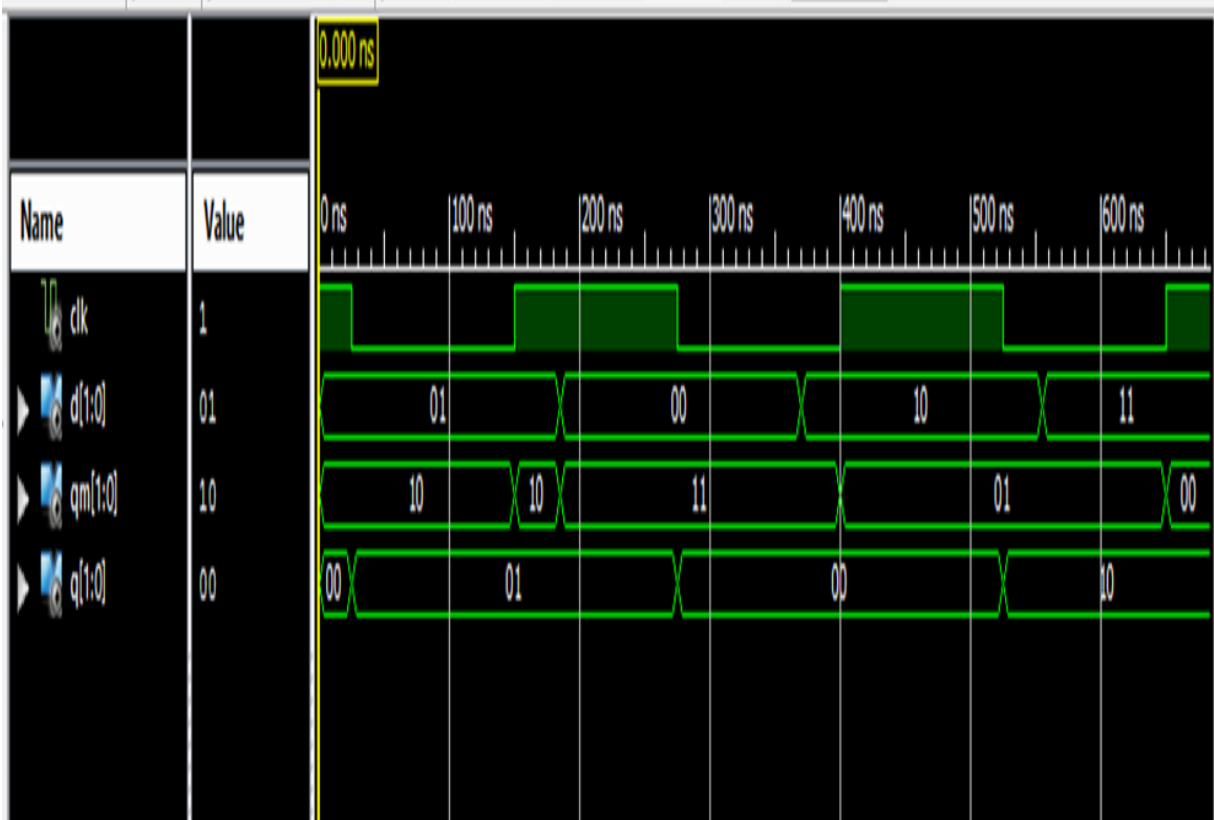


Fig 21. Behavioral simulation of SWS based Quaternary D flip flop

### 5.3 Integration with Binary logic

Quaternary logic can be easily converted to binary logic and vice versa using conversion circuits. Several methods have been proposed for binary to quaternary and vice versa converters [14,15,16,17]. If a complicated design is implemented using quaternary logic while the rest of the chip uses binary logic then such conversion circuits are very essential to integrate the different logic designs. This helps the quaternary and binary circuits to co-exist on the same die [7]. The binary to quaternary circuit shown in Figure 22 simply converts the 2 bit wide binary signal into 4 state analog signal by deploying an Analog multiplexer. The analog voltages are mapped to the 2 bit binary signals as shown in Table 5.

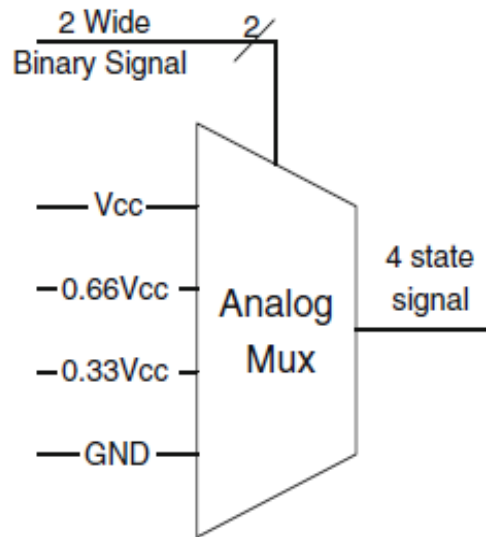


Fig 22. Binary to quaternary conversion circuit [7]

Table 5: Mapping of analog voltages to two bit binary logic

Analog signal	2 bit binary logic
Gnd	00
0.33 $V_{cc}$	01
0.66 $V_{cc}$	10
$V_{cc}$	11

The quaternary to binary circuit shown in Figure 23 uses a comparator circuit with some logic gates to produce the corresponding binary MSB and LSB digits. The Table 6 shows the binary LSB and MSB extraction from the quaternary analog signals. The reference voltages of the comparator can be adjusted according to the input analog voltages. The realization of this circuit may require many transistors but it can be used for integrating several quaternary logic circuits with binary logic on a chip.

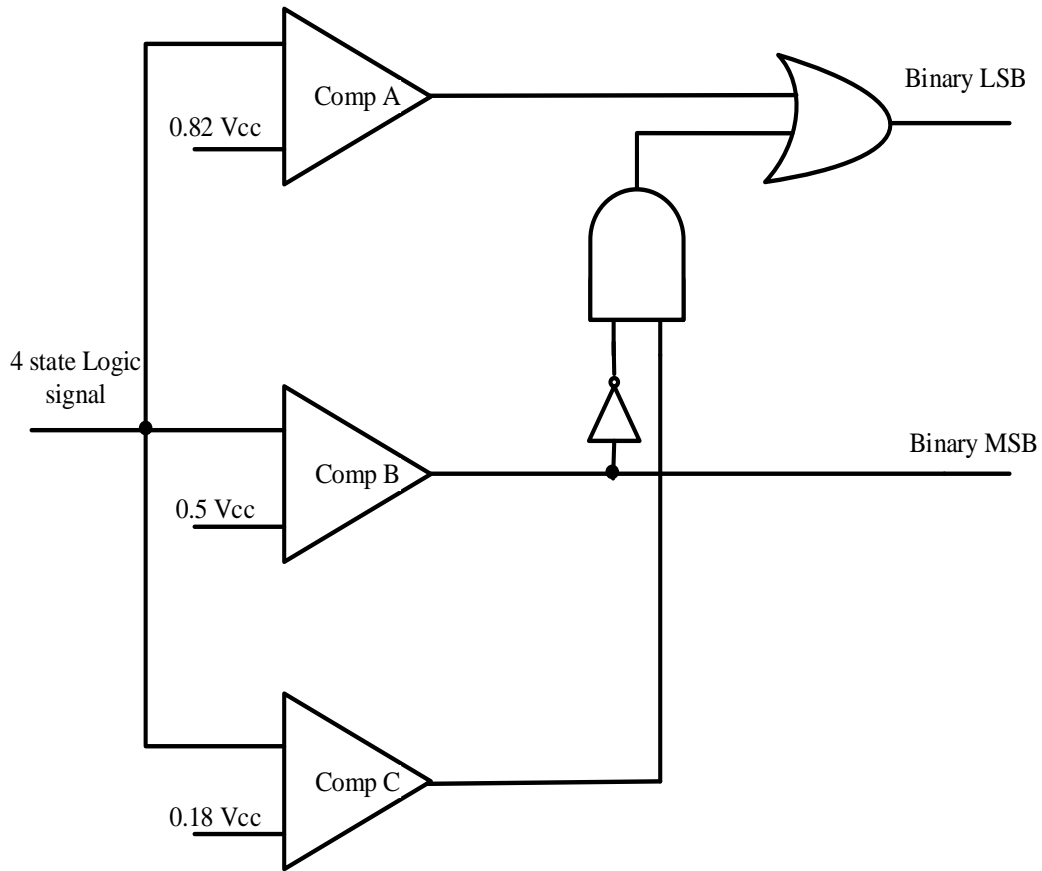


Fig 23. Quaternary to binary conversion circuit [7]

Table 6. Binary MSB and LSB outputs

4 state input	Comp A	Comp B	Comp C	Binary MSB	Binary LSB
Gnd	0	0	0	0	0
0.33Vcc	0	0	1	0	1
0.66Vcc	0	1	1	1	0
Vcc	1	1	1	1	1

### 5.3.1 Quaternary to Binary Converter using multiple-input floating gate MOSFETs

A quaternary to binary converter was presented in a paper [18]. The LSB and MSB separation from a quaternary digit is done using floating gate MOSFETs. Figure 24 and 25 show the MSB circuit diagram which gives logic '1' for  $V_{in} > 1.45$  V.

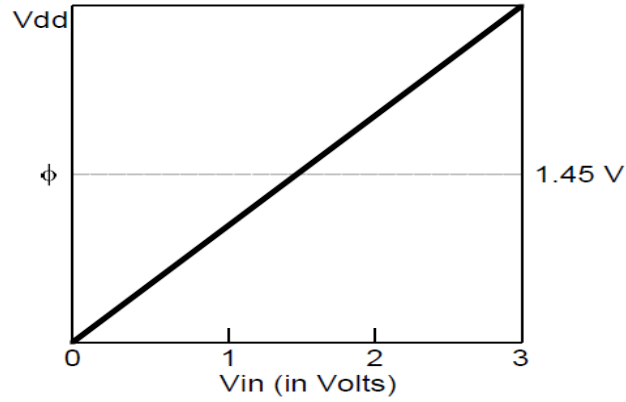


Fig 24. Floating gate potential diagram for the conversion of quaternary to MSB output [18]

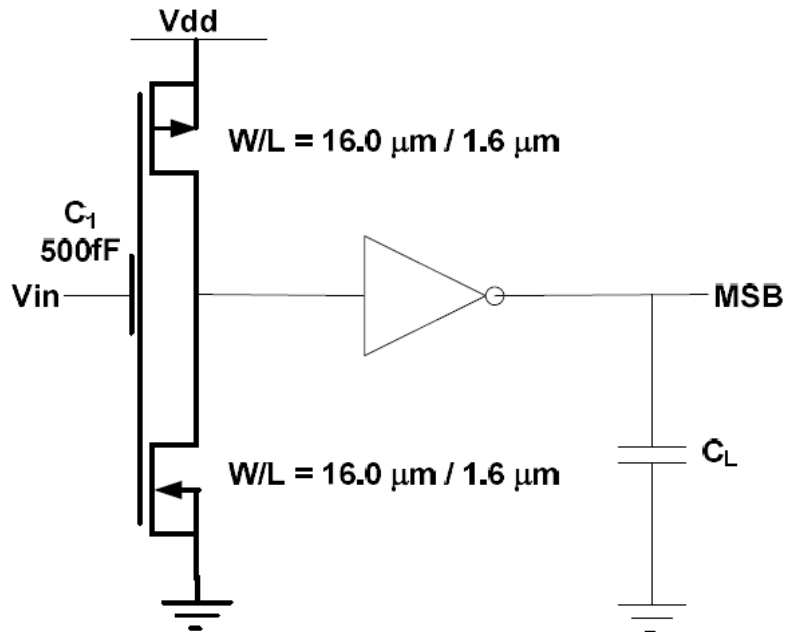


Fig 25. Circuit diagram for implementation of quaternary logic to binary logic – MSB using floating gate MOSFETs [18]

Similarly Figure 26 gives the floating point potential diagram (FPD) for extracting LSB from the quaternary signal [18]. The full circuit diagram for conversion quaternary digit to binary bits using floating gate MOSFETs is shown in Figure 28 [18].

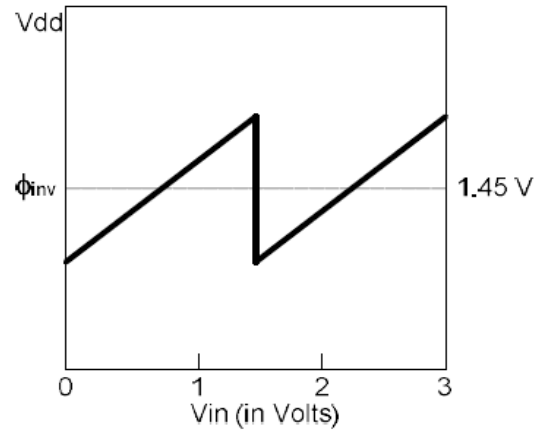


Fig 26. Floating gate potential diagram for conversion of quaternary to LSB output [18]

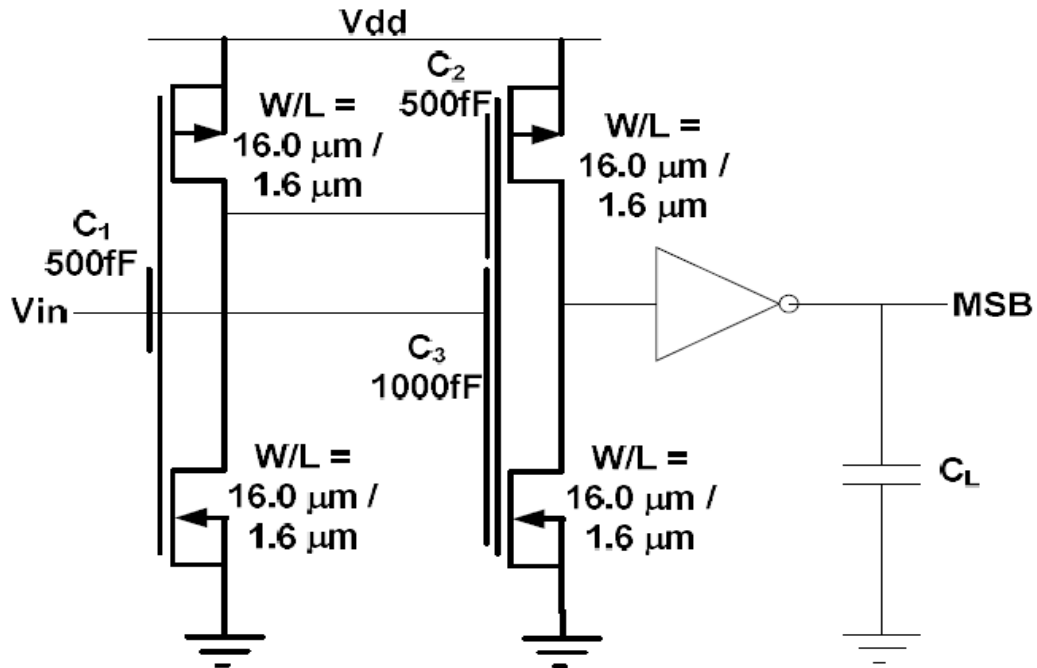


Fig 27. Floating point potential diagram for conversion of quaternary to LSB output Circuit diagram for implementation of quaternary to binary logic – LSB using floating gate MOSFETs [18]

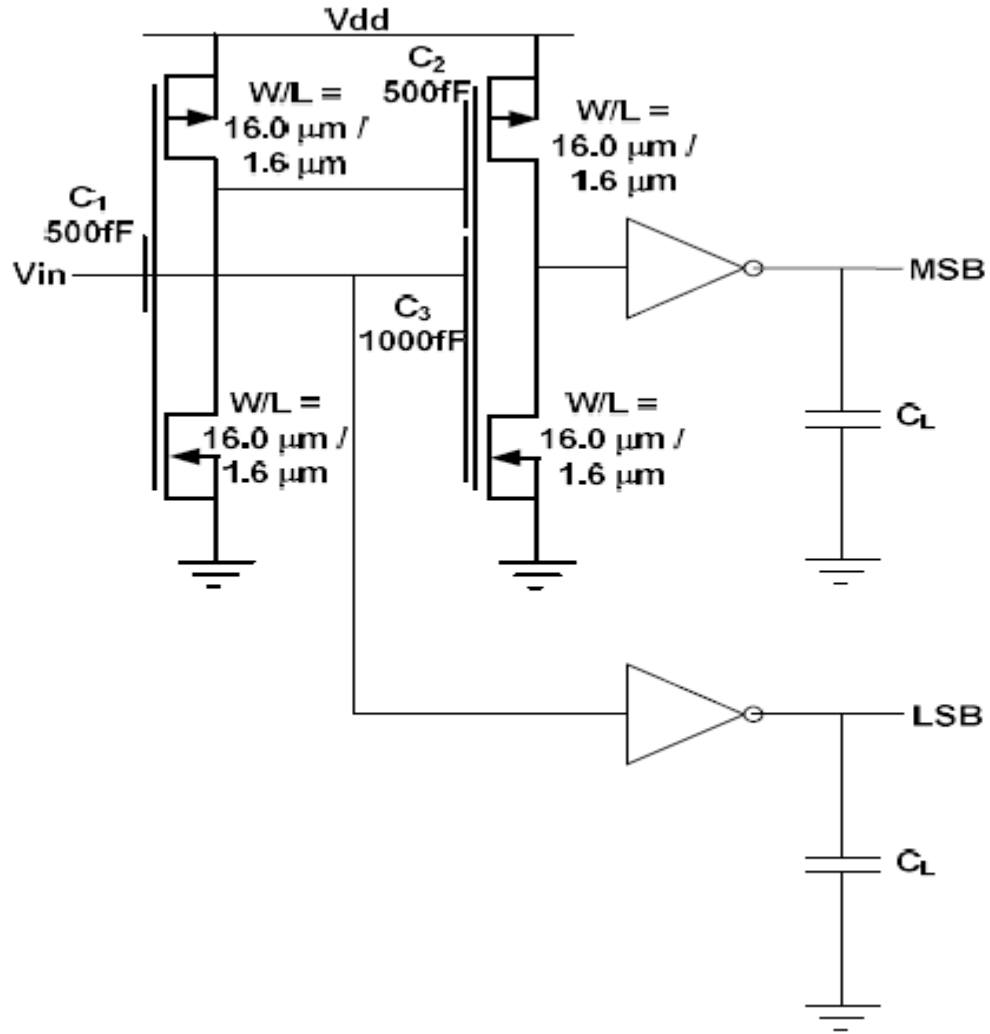
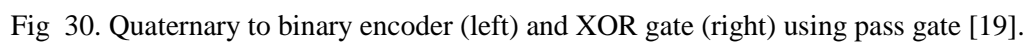
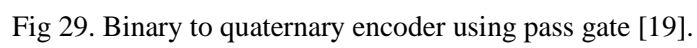


Fig 28.Full circuit diagram for conversion of quaternary (4-valued) logic to binary bits using floating gate MOSFETs [18]

### 5.3.2 Binary to Quaternary Convertor using Pass gates

The binary to convertor circuit diagram was presented in [19]. The LSB is used to select the appropriate voltage levels using pass transistor logic. The MSB signal drives the inverter to select the voltage from either the upper or lower branch to give a quaternary output Q0. The design was simulated for 0.13μm process technology using SPICE simulator and performed functionally well at 500MHz [19].





## **6. Applications of SWSFET based Sequential circuits**

In the previous chapters, SWSFET based latches and flip flop designs were demonstrated along with its simulations. Several other circuits can be designed using these sequential circuits and some of the common applications are counters and shift registers. An interesting dimension to these circuits will be the multi-valued logic of SWSFET which can increase the memory capacity of the system. The higher the radix, the more is the information that can be stored.

### **6.1 Counters**

A counter is a sequential circuit that goes through a certain sequence of states (like counting up or down) based on the input pulse. It can be an asynchronous or synchronous counter. The asynchronous counters will have the flip flops arranged in a way such that the output of one flip flop is fed as the clock of the following flip flop. The asynchronous counter (also called the ripple counter) is comparatively slow because each flip flop's clock is dependent on the output of the previous flip flop. Since there is always a non-zero propagation delay it slows down the system altogether. In the case of synchronous counters each flip flop is triggered by the same clock source, thus avoiding the cumulative delay found in asynchronous counters. The conventional counter is an n-bit binary counter. This has n flip flops and  $2^n$  states that go through the order from 0 to  $2^n - 1$ . The various uses of counters are counting, frequency divider circuits, sequencers for control logic in a processor, digital clock, time measurement, A to D converter, digital triangular wave generator and creating delays of a specific duration.

#### **6.1.1 Multi-valued Counters**

In multi-valued logic domain several counters have been reported. Tai haur kuo in paper [21] describes the use of resonant tunneling diodes (RTDs) for multi-valued counters. This counter was implemented using a unique state-dependent current source to successively trigger RTD-based counter [21]. In another paper [22] J. G. Lomsdalen demonstrates a multi-valued counter based on recharged semi floating gate structures. By using a clock signal as an input, the counter starts counting up or down depending on the sampled value and the phase of the clock signal.

The multi-valued counters will use ‘N’ counters to count upto  $m^N$ . Here ‘m’ represents the multi-valued logic used. So for a quaternary logic, when two flip flops are cascaded the count goes to 16 ( $4^2$ ) steps. In binary logic the same implementation (mod 16) counter would require four flip flops.

Table 7. State table of Quaternary Up-counter [11]

Present state		Next state	
Q1	Q0	Q1+	Q0+
0	0	0	1
0	1	0	2
0	2	0	3
0	3	1	0
1	0	1	1
1	1	1	2
1	2	1	3
1	3	2	0
2	0	2	1
2	1	2	2
2	2	2	3
2	3	3	0
3	0	3	1
3	1	3	2
3	2	3	3
3	3	0	0

## 6.2 Shift Registers

The shift register stores data and also moves data. Since it stores data it can be implemented using flip-flops. The flip flop operation has already been discussed in an earlier chapter. So when a clock edge is detected the flip flop stores the value of the input data. In a conventional binary type, one flip flop is required for each bit that needs to be stored. The number of individual flip flops that constitute a single shift register is ascertained by the number of bits to be stored. Therefore if four bits are to be stored then four flip-flops are needed. Each flip flop stores one bit which means each stage of the register stores one bit. The data can be fed in or out of the register serially (left or the right direction) or in parallel.

### 6.2.1 Types of Shift Registers

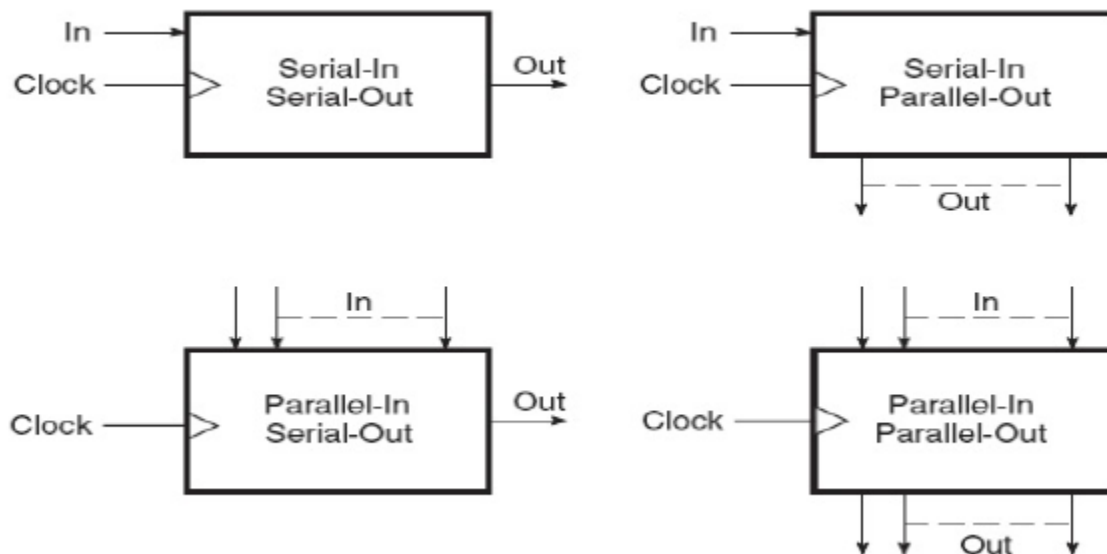


Fig 31. Shift register in different modes [23].

Shift registers can be classified into four different types. The Serial Input Serial Output register shifts data in or out one at a time in left or right direction whereas the Serial Input Parallel Output register loads data serially and outputs in parallel format. Next, the Parallel Input Serial Output register feeds the data all at a time but shifts the output one at a time and Parallel Input Parallel Output register inputs data and shifts simultaneously in one clock pulse.

### 6.2.2 Multi-valued Shift Registers

A multiple-valued shift register can be constructed by cascading multi-valued flip flops. A three-valued shift register has been reported earlier [20]. This uses a three-valued D flip flop built from InGaAs based multiple-junction surface tunnel transistors (MJSTT). The shift register constructed by cascading two D flip flops has to maintain the input voltage each time clock goes to zero because of gate leakage current. To mitigate this leakage, a level shift circuit of the source-follower type consisting of two depletion-type HJFETs was inserted between the two D flip flop circuits [20]. By using a quaternary D flip flop two bits can be stored in one register and by cascading two of those flip flops will result in a four bit shift register. The same implementation using conventional binary logic would require four flip flops.

A simple Serial Input Serial Output shift register can be designed using a quaternary flip flop. The block diagram in Figure 32 shows four serially connected negative flip flops that are capable of handling 8 bits because each flip flop can store two bits.

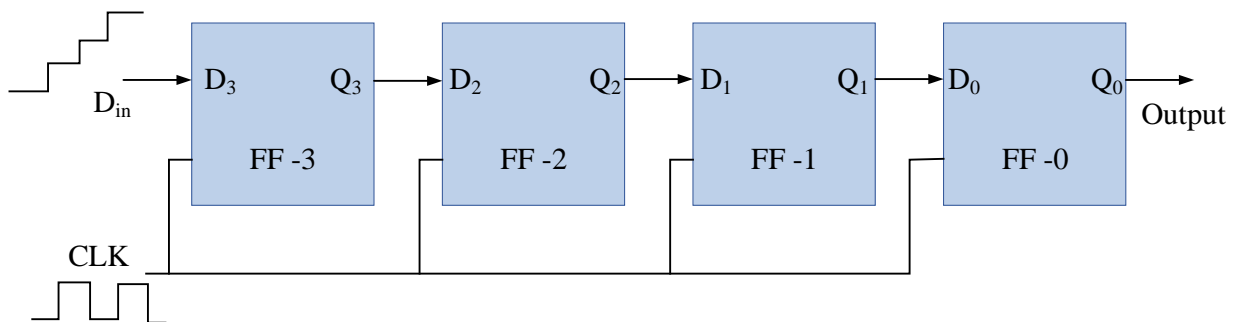
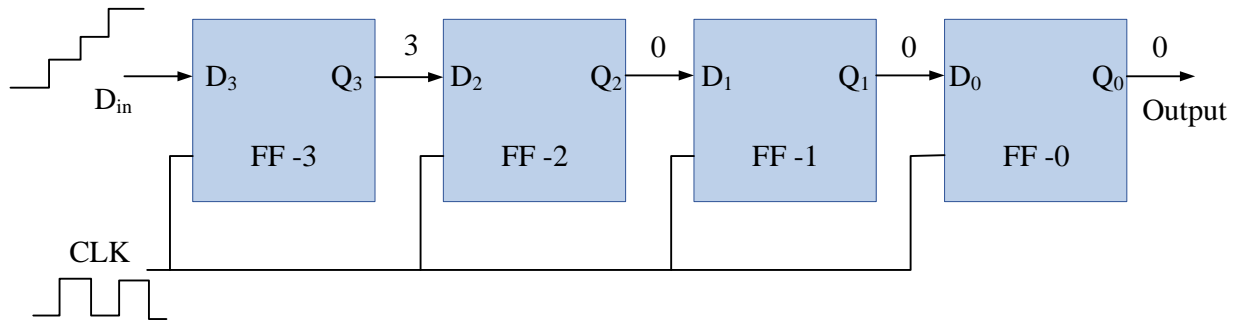
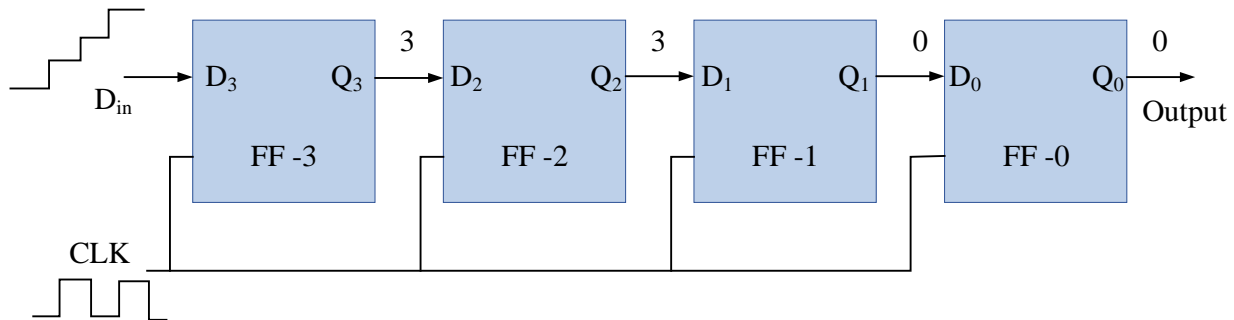


Fig 32. 8 bit Serial Input Serial Output Shift register

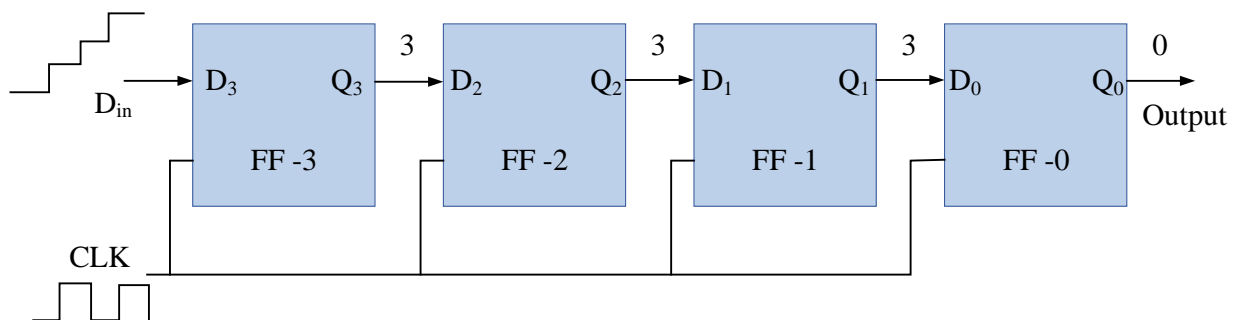
The flip flops are initially in the reset condition where signals  $Q_3$   $Q_2$   $Q_1$   $Q_0$  are equal to 0000. If a quaternary input '3333' is applied to the input D, the data is passed on serially starting from the LSB. On the first falling edge of clock, data is clocked into FF-3 thus giving '3000'.



Next bit is applied to the input and on the second falling edge of clock the stored data becomes '3300'.



Consecutively the next bit is applied and on the next negative pulse  $Q_3$   $Q_2$   $Q_1$   $Q_0$  becomes '3330'.



On the fourth falling clock edge, the stored data in the register is '3333'.

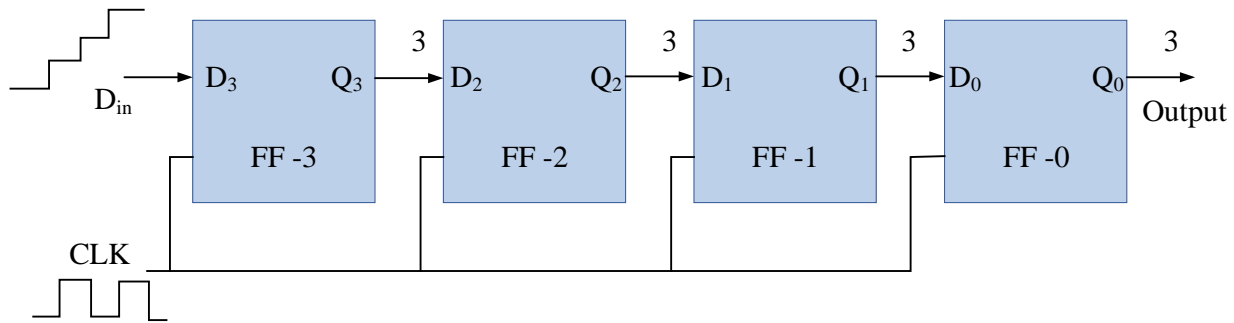


Table 8: Truth table of 8 bit Serial Input Serial Output Shift register

CLK	$D_{in} = D_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	$Q_0$
		0	0	0	0
↓	3	3	0	0	0
↓	3	3	3	0	0
↓	3	3	3	3	0
↓	3	3	3	3	3

—————→ Direction of data movement

It requires four clock cycles to shift the quaternary input '3333' serially. The binary equivalent of '3333' is '11111111' which has a length of 8 bits and it could be implemented with only four quaternary flip flops. In the conventional CMOS technology, eight flip flops will be required and the number of clock cycles will also be doubled. By using quaternary logic, there is a reduction in device count and number of clock cycles.

## 7. Conclusion

The implementation of binary logic designs and sequential circuits using SWSFET has been successful. SR latch and D flip flop are the fundamental blocks of sequential circuits so several other circuits can be designed using these basic units. As the number of devices decreases, the complexity of wiring is reduced and so is the die area. Also it could lower the power consumption and improve the efficiency of the device [5]. The higher radix logic designs using multi-channel SWSFETs show a pronounced reduction in the transistor count. Even though multi-valued logic is not prevalent much in the existing digital designs, SWSFET has good prospects for future multi-valued logical designs.

### 7.1 Comparison with CMOS technology

The logic cells designed using SWSFETs use lesser number of transistors than the CMOS technology. It can be seen from the bar chart in Fig.33 that the number of transistors used in the conventional CMOS two bit logic design is much higher than the SWSFET logic design.

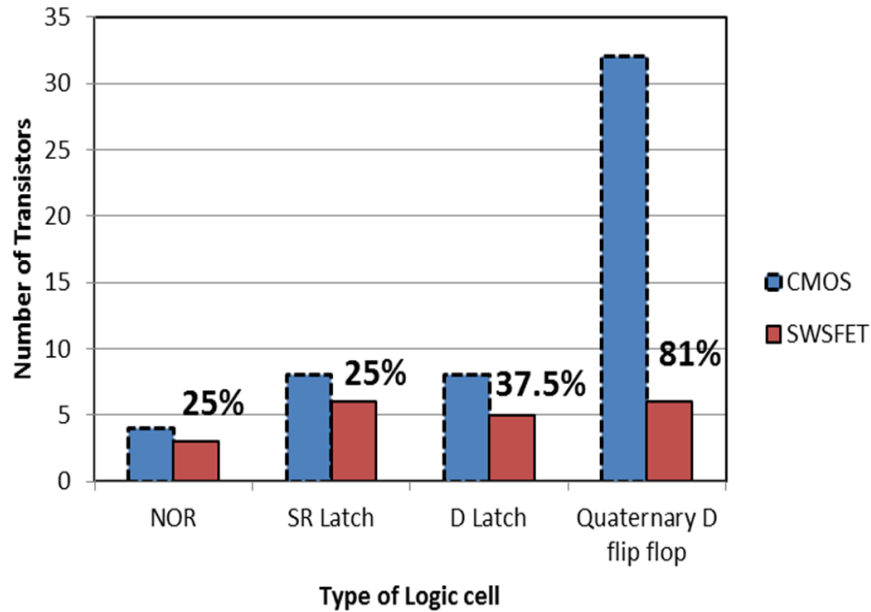


Fig 33. Percentage decrease in number of transistors between CMOS and SWSFET technology.

## **7.2 Suggestions for future work**

SWSFET model was created to verify the functionality of device in several logic circuits. The quantum effects of the device have to be incorporated in the model to simulate a more precise functioning of the device. The most interesting dimension of these SWSFETs is the multi-valued logic but there are several challenges pertinent to fabrication in sub nm regime and realization of these circuits. The voltage separation between the different levels in the multi-valued voltages is very small. So the noise margin has to be improved which is poor in any multi-valued signal.

The multi-valued structures are compact structures with fewer interconnections and higher memory capacity. There could be lower power consumption because fewer blocks are used. However actual power measurements are require to gauge the efficiency of the circuit. Measurements like energy-delay product, a metric of energy efficiency can also be done.



## 8. References

1. F. C. Jain, E. Suarez, M. Gogna, F. Alamoody, D. Butkiewicz, R. Hohner, T. Liaskas, S. Karmakar, P. -Y. Chan, B. Miller, J. Chandy, and E. Heller, *J. of Elec. Mater.*, 38, 8, pp. 1574-1578 (2009).
2. Quantum dot channel (QDC) quantum dot gate transistors, memories and other devices, US Patent, Application Number: 20120280208, August 11 (2012).
3. F. C. Jain, J. Chandy, B. Miller, E-S. Hasaneen, and E. Heller, *Int. J. High Speed Electronics and Systems*, 20, 3, pp. 641-652 (2011)
4. H.C. Lin, *24th IEEE International Symposium on Multiple-Valued Logic* (Boston, Massachusetts, USA: IEEE Computer Society), pp. 188 (1994).
5. P. Gogna, M. Lingalugari, J. Chandy, F.C. Jain, E. Heller, and E. Hasaneen, *Lester Eastman Conference on High Performance Devices (LEC), IEEE Conference Publication* (2012).
6. F.C. Jain, B. Miller., E. Suarez., P.-Y. Chan, S. Karmakar, F. Al-Amoody, M. Gogna, J. Chandy, and E. Heller, *J. of Elec. Mater.*, 40, pp.1717 (2011).
7. P. Gogna, M. Lingalugari, J. Chandy, E. Heller, E-S. Hasaneen, and F. Jain, *Int. J. VLSI design & Communication Systems*, 3, 6 (2012).
8. E. Suarez., P.-Y. Chan, M. Gogna, J.E.Ayers, E.Heller and F.C.Jain, *Int. J. High Speed Electronics and Systems*, 23, 1&2 1450013(2014).
9. S.Karmakar, *International Journal of VLSI design & Communication Systems (VLSICS)*, 4, 3, June 2013.
10. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, *Digital Integrated Circuits*, II edition, pp 271-315, (2003).
11. K.S. Vasundara Patel and K.S. Gurumurthy, *Int. J. Comput. Theory Eng.* 2, 1793 (2010).
12. Thurman A.Irving, Sajjan G Shiva, H Troy Nogle, *IEEE Transactions on Computers* , 25,3 ,pp 237 (1976).
13. L.Sintonen, *IEEE Transactions on Computers*, 26,3, pp.292,(1977).
14. N.R. Shanbhag, D. Nagchoudhuri, R.E. Siferd, G.S. Vishweswaran, Quaternary logic circuits in 2 mm CMOS technology, *IEEE J. Solid-State Circuits* 25 (1990) 790–799.
15. J.L. Mangin, K.W. Current, Characteristics of prototype CMOS quaternary logic encoder decoder circuits, *IEEE Trans. Comput.* C-35 (1986) 157–161.
16. K.W. Current, Current-mode multiple-valued logic circuits, *IEEE J. Solid-State Circuits* 29 (1994) 95–107.

17. I.M. Thoidis, D. Soudris, I. Karafyllidis, A. Thanailakis, "The design of low power multiple valued logic encoder and decoder circuits", *Proceedings of the Sixth IEEE International Conference on Electronics, Circuits and Systems*, Vol. 3, September 1999, pp. 1623–1626.
18. Srivastava, H.N. Venkata, "Quaternary to binary bit conversion CMOS integrated circuit design using multiple-input floating gate MOSFETS", *INTEGRATION, the VLSI journal* 36 (2003) 87–10.
19. Jean-Marc Philippe, S'ébastien Pillement, Olivier Sentieys, "A Low-Power and High-Speed Quaternary Interconnection Link using Efficient Converters", *IEEE International Symposium on Circuits and Systems*, May 2005, pp 4689 - 4692 Vol. 5
20. Tetsuya Uemura and Toshio Baba, *IEEE Conference Publication* 49, 8, (2002).
21. Tai haur kuo, Hung Chang Lin, Robert C. Potter, and Dave Schupe, *IEEE Transaction of computers*, 42,1, (1993).
22. Johannes G.Lomsdalen , R.Jensen, and Y.Berg, *IEEE Design and Diagnostics of Electronic Circuits and systems*, pp. 245-247, 2006
23. Mohammad A.S Bhuiyan, Hasrul N.B Rosly, M.I.Reaz, K.N.Minhad, Hafizah Husain, "Advances on CMOS Shift registers for digital data storage", *Telkomnika Indonesian Journal of Electrical Engineering*, Vol 12, No.5, May 2014 pp 3849-3862.